



**What Is Claimed Is:**

1. A MOS (metal on semiconductor transistor) structure for ESD protection, comprising:
  - an active region, defined on a substrate of a second-type conductivity;
  - a channel region separating the active region into a first drain/source region and a second drain/source region;
  - at least one first island, formed on the first drain/source region and having a first conductive segment and a first gate oxide segment of the first thickness, the first conductive segment being stacked on the first gate oxide segment;
  - a doped drain region of a first-type conductivity in the first drain/source region, defined substantially by a field oxide region, the channel region and the at least one first island; and
  - a breakdown-enhanced layer, formed in the first drain/source region and contacting the doped drain region, to reduce a breakdown voltage across the doped drain region and the substrate.
2. The MOS structure as claimed in claim 1, wherein the MOS structure has, within the active region, two breakdown-enhanced layers with the same depth and the same dosage, and one of the breakdown-enhanced layers is inside the first drain/source region while another is outside the first drain/source region.



3. The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer has the first-type conductivity.

4. The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer also forms pocket-implanted structures of internal MOS.

5. The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer has the second-type conductivity.

6. The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer also forms anti-punch-through structures of internal MOS.

7. The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer is formed under the doped drain region.

8. The MOS structure as claimed in claim 1, wherein the channel region has a gate structure consisting of a second conductive segment and a second gate oxide segment, the second conductive segment being stacked on the second gate oxide segment.

9. The MOS structure as claimed in claim 8, wherein the second gate oxide and the first gate oxide have the same thickness.

10. The MOS structure as claimed in claim 8, wherein the second gate oxide and the first gate oxide have different thicknesses.



1 11. The MOS structure as claimed in claim 10, wherein the second  
2 gate oxide is thicker than the first gate oxide.

1 12. The MOS structure as claimed in claim 11, wherein the  
2 breakdown-enhanced layer is formed at the at least one first  
3 island breakdown-enhanced layer and an internal-circuit MOS  
4 transistor with the first gate oxide thickness  
5 simultaneously.

13. The MOS structure as claimed in claim 1, wherein the  
breakdown-enhanced layer is not formed in the second  
drain/source region.

14. The MOS structure as claimed in claim 1, wherein the channel  
region has a field oxide stacked on the substrate.

15. An electrostatic discharge protection device on a substrate  
of a second-type conductivity, comprising:

a source region of a first-type conductivity, coupled to a  
power rail;

a drain region of the first-type conductivity, coupled to a  
pad via a contact;

a first gate structure placed between the source region and  
the drain region, for controlling electric connection  
between the drain region and the source region; and

a second gate structure substantially surrounded by the drain  
region, for distancing the contact from the first gate  
structure;



13            wherein the first gate structure and the second gate  
14            structure receives different implant treatments.

1        16.The electrostatic discharge protection device as claimed in  
2            claim 15, wherein the second gate structure distances the  
3            contact from the first gate structure.

1        17.The electrostatic discharge protection device as claimed in  
2            claim 15, wherein the first gate structure includes an  
3            adjacent first doped junction; the second gate structure  
4            includes an adjacent second doped junction; and the first and  
5            second doped junctions have different doping profiles.

1        18.The electrostatic discharge protection device as claimed in  
2            claim 15, wherein a gate oxide of the first gate structure  
3            and a gate oxide of the second gate structure have the same  
4            thickness.

1        19.The electrostatic discharge protection device as claimed in  
2            claim 15, wherein a gate oxide of the first gate structure  
3            and a gate oxide of the second gate structure have different  
4            thicknesses.

1        20.The electrostatic discharge protection device as claimed in  
2            claim 15, wherein the gate oxide of the first gate structure  
3            is thicker than the gate oxide of the second gate structure.

1        21.The electrostatic discharge protection device as claimed in  
2            claim 15, wherein the second gate structure receives  
3            breakdown-enhanced implantation while the first gate



structure is sheltered from the breakdown-enhanced  
implantation.

22. The electrostatic discharge protection device as claimed in  
claim 21, wherein the breakdown-enhanced implantation is  
pocket implantation to form pocket-implanted structures.

23. The electrostatic discharge protection device as claimed in  
claim 21, wherein the breakdown-enhanced implantation is  
anti-punch-through implantation.

24. The electrostatic discharge protection device as claimed in  
claim 21, wherein the breakdown-enhanced implantation is to  
form a breakdown-enhanced layer under the drain region.

25. The electrostatic discharge protection device as claimed in  
claim 24, wherein the breakdown-enhanced layer has the  
second-type conductivity.

26. An electrostatic discharge protection device, comprising:  
an active region on a substrate of a second-type  
conductivity;  
a first gate structure and a second gate structure, both being  
placed on the active region;  
at least one drain region of a first-type conductivity and  
one source region of the first-type conductivity, defined  
and separated by either the first gate structure or the  
second gate structure; and



10 a breakdown-enhanced layer, formed within the drain region  
11 to reduce a breakdown voltage across the drain region and  
12 the substrate.

1 27. The electrostatic discharge protection device as claimed in  
2 claim 26, wherein the at least one drain region and one source  
3 region are respectively coupled to a pad and a power rail.

1 28. The electrostatic discharge protection device as claimed in  
2 claim 26, wherein the breakdown-enhanced layer is not present  
3 within the source region

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29. The electrostatic discharge protection device as claimed in  
claim 26, wherein a gate oxide of the first gate structure  
is thicker than a gate oxide of the second gate structure.

30. The electrostatic discharge protection device as claimed in  
claim 26, wherein the first gate structure separates the  
active region into two drain/source regions as well as the  
second gate structure does.

1 31. The electrostatic discharge protection device as claimed in  
2 claim 26, wherein the breakdown-enhanced layer has the  
3 first-type conductivity.

1 32. The electrostatic discharge protection device as claimed in  
2 claim 31, wherein the breakdown-enhanced layer also forms  
3 pocket-implanted structures of internal MOS.



1 33.The electrostatic discharge protection device as claimed in  
2 claim 26, wherein the breakdown-enhanced layer has the  
3 second-type conductivity.

1 34.The electrostatic discharge protection device as claimed in  
2 claim 26, wherein the breakdown-enhanced layer also forms  
3 anti-punch-through structures of internal MOS.

1 35.The electrostatic discharge protection device as claimed in  
2 claim 26, wherein the breakdown-enhanced layer is formed  
under the doped drain region.

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